IN THE CLAIMS:

Claims 1-16 (Cancelled)

Claim 17 (Original) A semiconductor memory device comprising:

a memory cell array which includes a plurality of sub-arrays, a plurality of sub-row decoders provided between said plurality of respective sub-arrays, for driving a plurality of sub-word lines, a main row decoder disposed on one-end side of said plurality of sub-arrays in a sub-word line direction, and a plurality of main-block selecting lines for respectively supplying outputs of said main row decoder to said sub-row decoders;

wherein said plurality of sub-arrays each include said plurality of sub-word lines, a plurality of bit lines, a plurality of plate lines and a plurality of memory cell blocks, said plurality of sub-arrays are arranged in said sub-word line direction, a metal interconnection used for forming said plate lines and a metal interconnection used for forming said main-block selecting lines are formed by metal interconnection layers at the same level, said memory cell blocks each include a plurality of series-connected memory cells and at least one selection transistor serially connected to at least one end of said series-connected portion, one end of each of said memory cell blocks is coupled to a corresponding one of said bit lines, the other end thereof is connected to a corresponding one of said plate lines, a gate terminal of each cell transistor is connected to a corresponding one of said sub-word lines, said memory cell includes said cell transistor and a ferroelectric capacitor connected between source and drain terminals of said cell transistor, and a metal interconnection used for parallel connection of said cell transistor and said ferroelectric capacitor is formed by a metal interconnection layer formed at the same level as said plate lines and said main-block selecting lines.

Claims 18-20 (Cancelled)